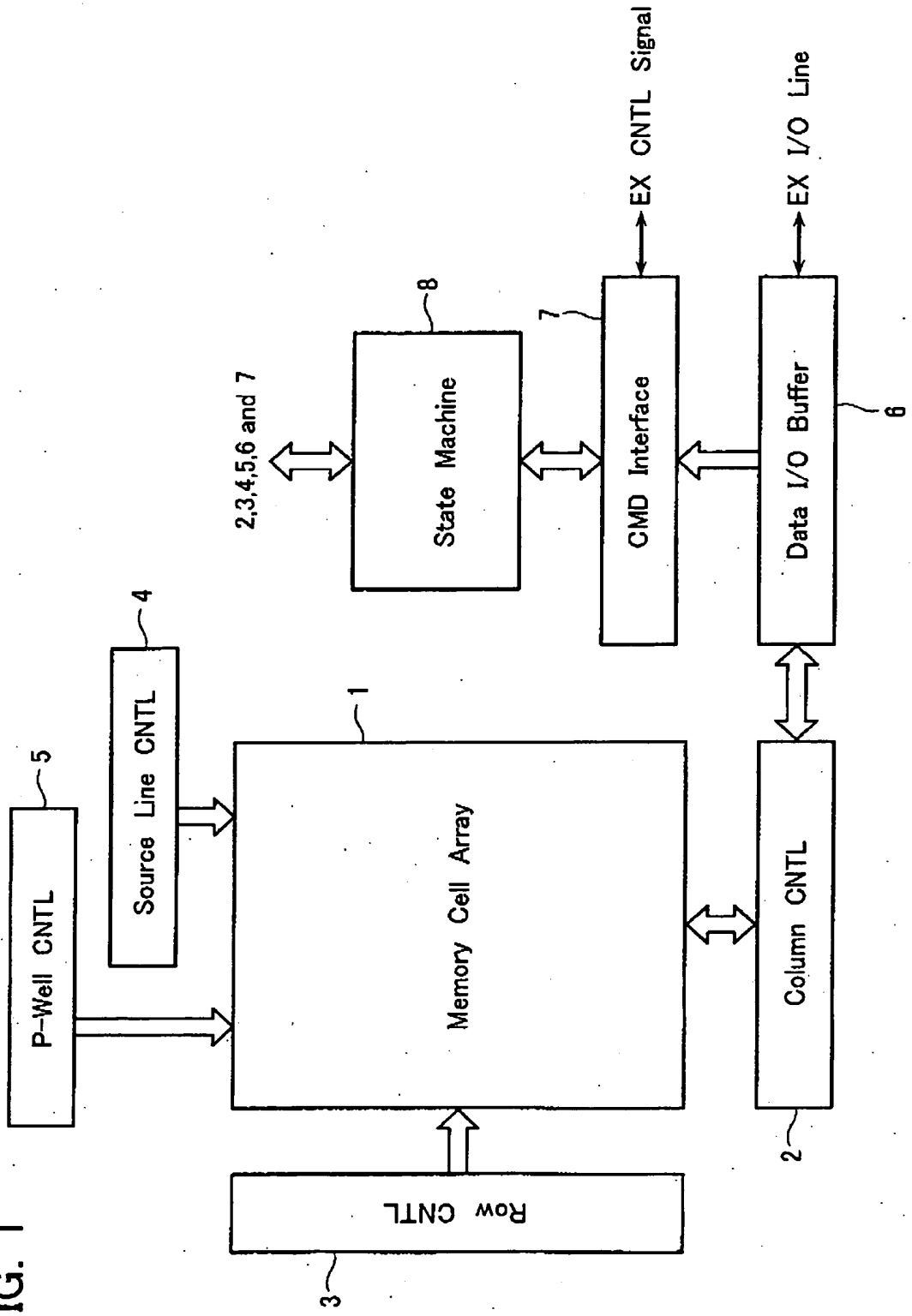
EX CNTL Signal
EX I/O Line
8
7
2,3,4,5,6 and 7
State Machine
CMD Interface
Data I/O Buffer
6
4
1
5
Source Line CNTL
Memory Cell Array
P-Well CNTL
Column CNTL
2
Row CNTL
3

FIG. 1

FIG. 2

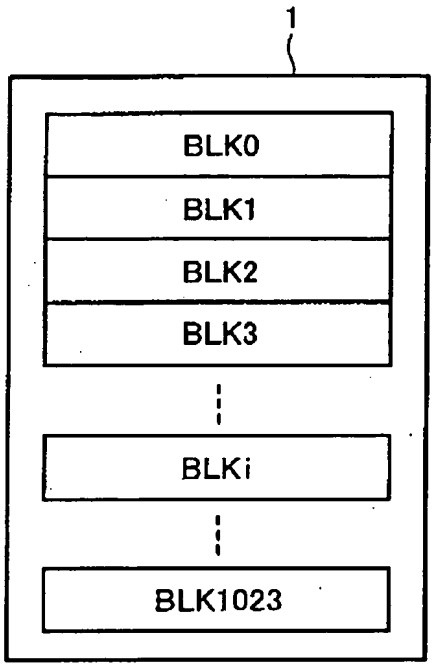

FIG. 3

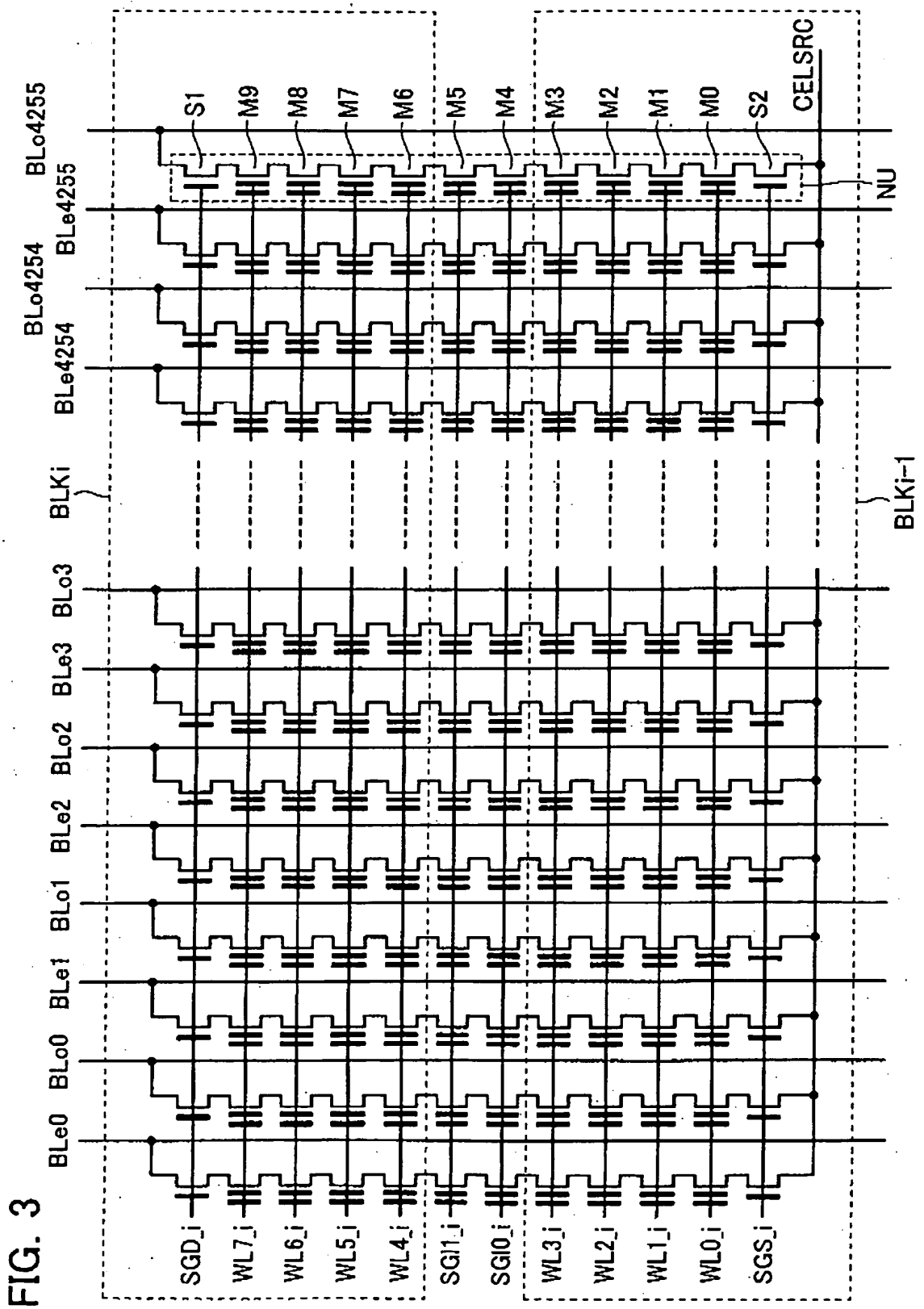
BLo4255
BLe4255
BLo4254
BLe4254
BLKi
BLKi-1
S1
M9
M8
M7
M6
M5
M4
M3
M2
M1
M0
S2
CELSRC
NU
BLo3
BLe3
BLo2
BLe2
BLo1
BLe1
BLo0
BLe0
SGD_i
WL7_i
WL6_i
WL5_i
WL4_i
SGI1_i
SGI0_i
WL3_i
WL2_i
WL1_i
WL0_i
SGS_i

FIG. 4

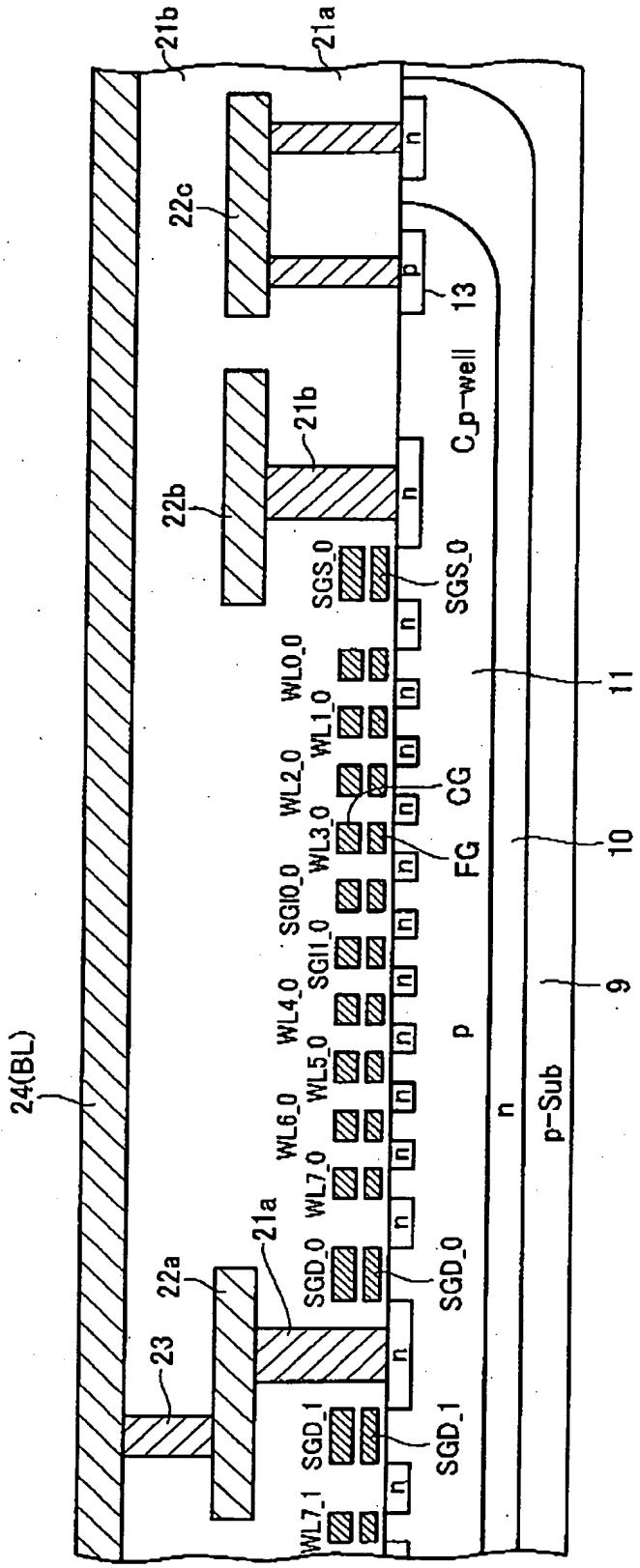
21b
21a
22c
13
C_p-well
21b
22b
SGS_0
SGS_0
WL0_0
WL1_0
WL2_0
WL3_0
CG
FG
SGI0_0
SGI1_0
WL4_0
WL5_0
WL6_0
WL7_0
11
10
9
24(BL)
p
n
p-Sub
21a
22a
23
SGD_0
SGD_0
SGD_1
SGD_1
WL7_1

FIG. 5

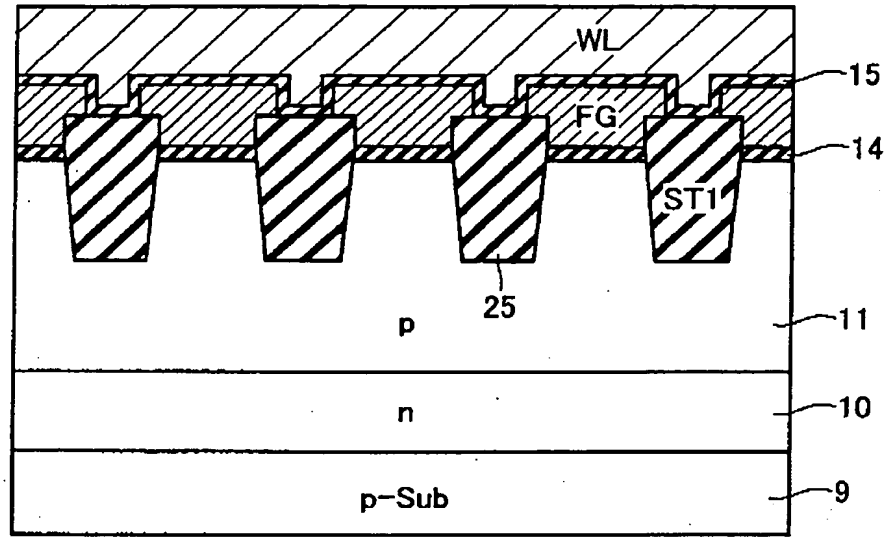

FIG. 6

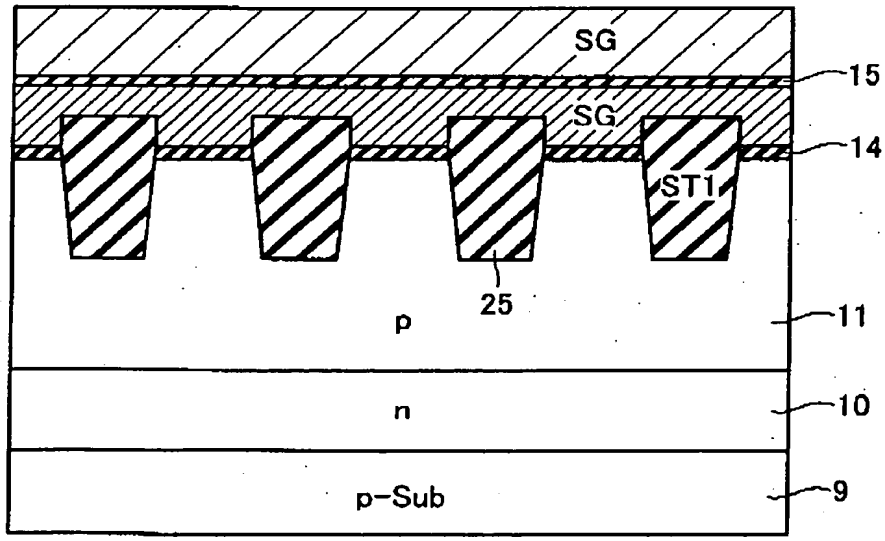

FIG. 7

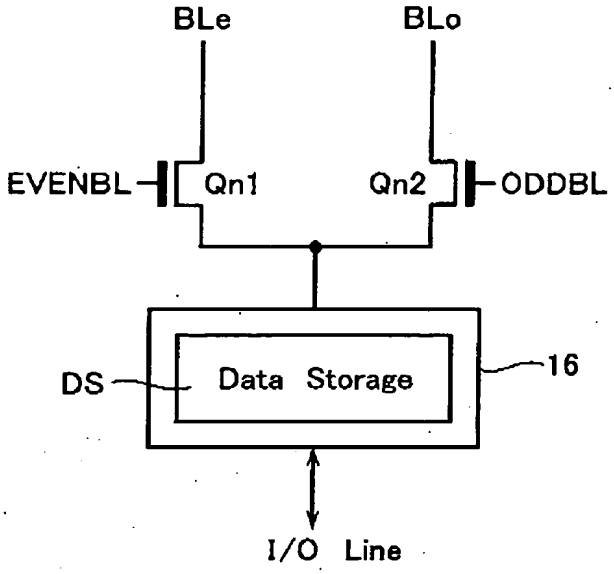
BLe
BLo
EVENBL
Qn1
Qn2
ODDBL
DS
Data Storage
16
I/O Line

FIG. 8

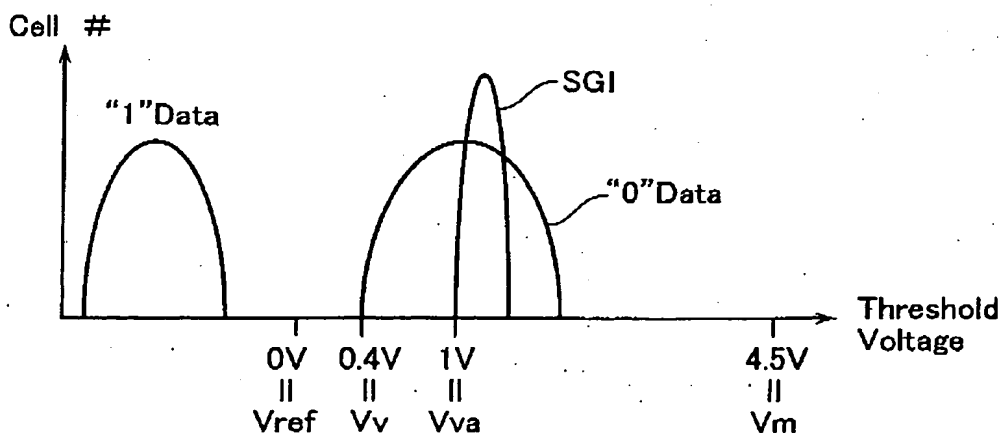
Cell #
"1"Data
SGI
"0"Data
Threshold Voltage
0V
||
Vref
0.4V
||
Vv
1V
||
Vva
4.5V
||
Vm

FIG. 9

		Erase	"0" Write	"1" Write	Read	Write-Verify
	BLe	Floating	0V	Vdd	H or L	H or L
	BLo	Floating	Vdd	Vdd	0V	0V
	SGD	Floating	Vdd	Vdd	4.5V	4.5V
BLKi	WL7	Floating	4.5V	4.5V	4.5V	4.5V
	WL6	Floating	4.5V	4.5V	4.5V	4.5V
	WL5	Floating	4.5V	4.5V	4.5V	4.5V
	WL4	Floating	4.5V	4.5V	4.5V	4.5V
	SGI1	Floating	Vdd	Vdd	4.5V	4.5V
	SGI0	Floating	Vdd	Vdd	4.5V	4.5V
BLKi-1	WL3	0V	10V	10V	4.5V	4.5V
	WL2	0V	10V	10V	4.5V	4.5V
	WL1	0V	Vpgm	Vpgm	0V	0.4V
	WL0	0V	10V	10V	4.5V	4.5V
	SGS	Floating	0V	0V	4.5V	4.5V
	CELSRC	Floating	0V	0V	0V	0V
	C-p-well	20V	0V	0V	0V	0V

FIG. 10

		Erase	"0" Write	"1" Write	Read	Write-Verify
	BLe	Floating	0V	Vdd	H or L	H or L
	BLo	Floating	Vdd	Vdd	0V	0V
	SGD	Floating	Vdd	Vdd	4.5V	4.5V
BLKi	WL7	0V	10V	10V	4.5V	4.5V
	WL6	0V	10V	10V	4.5V	4.5V
	WL5	0V	Vpgm	Vpgm	0V	0.4V
	WL4	0V	10V	10V	4.5V	4.5V
	SGI1	Floating	0V	0V	4.5V	4.5V
	SGI0	Floating	0V	0V	4.5V	4.5V
BLKi-1	WL3	Floating	4.5V	4.5V	4.5V	4.5V
	WL2	Floating	4.5V	4.5V	4.5V	4.5V
	WL1	Floating	4.5V	4.5V	4.5V	4.5V
	WL0	Floating	4.5V	4.5V	4.5V	4.5V
	SGS	Floating	0V	0V	4.5V	4.5V
	CELSRC	Floating	0V	0V	0V	0V
	C-p-well	20V	0V	0V	0V	0V

FIG. 11

		Erase	"0" Write	"1" Write	Read	Write-Verify
	BLe	Floating	0V	Vdd	H or L	H or L
	BLo	Floating	Vdd	Vdd	0V	0V
	SGD	Floating	Vdd	Vdd	4.5V	4.5V
BLKi	WL7	Floating	10V	10V	4.5V	4.5V
BLKi	WL6	Floating	10V	10V	4.5V	4.5V
BLKi	WL5	Floating	10V	10V	4.5V	0.4V
BLKi	WL4	Floating	10V	10V	4.5V	4.5V
	SGI1	0V	Vpgm	Vpgm	0V	1V
	SGI0	0V	10V	10V	4.5V	4.5V
BLKi-1	WL3	Floating	10V	10V	4.5V	4.5V
BLKi-1	WL2	Floating	10V	10V	4.5V	4.5V
BLKi-1	WL1	Floating	10V	10V	4.5V	4.5V
BLKi-1	WL0	Floating	10V	10V	4.5V	4.5V
	SGS	Floating	0V	0V	4.5V	4.5V
	CELSRC	Floating	0V	0V	0V	0V
	C-p-well	20V	0V	0V	0V	0V

FIG. 12

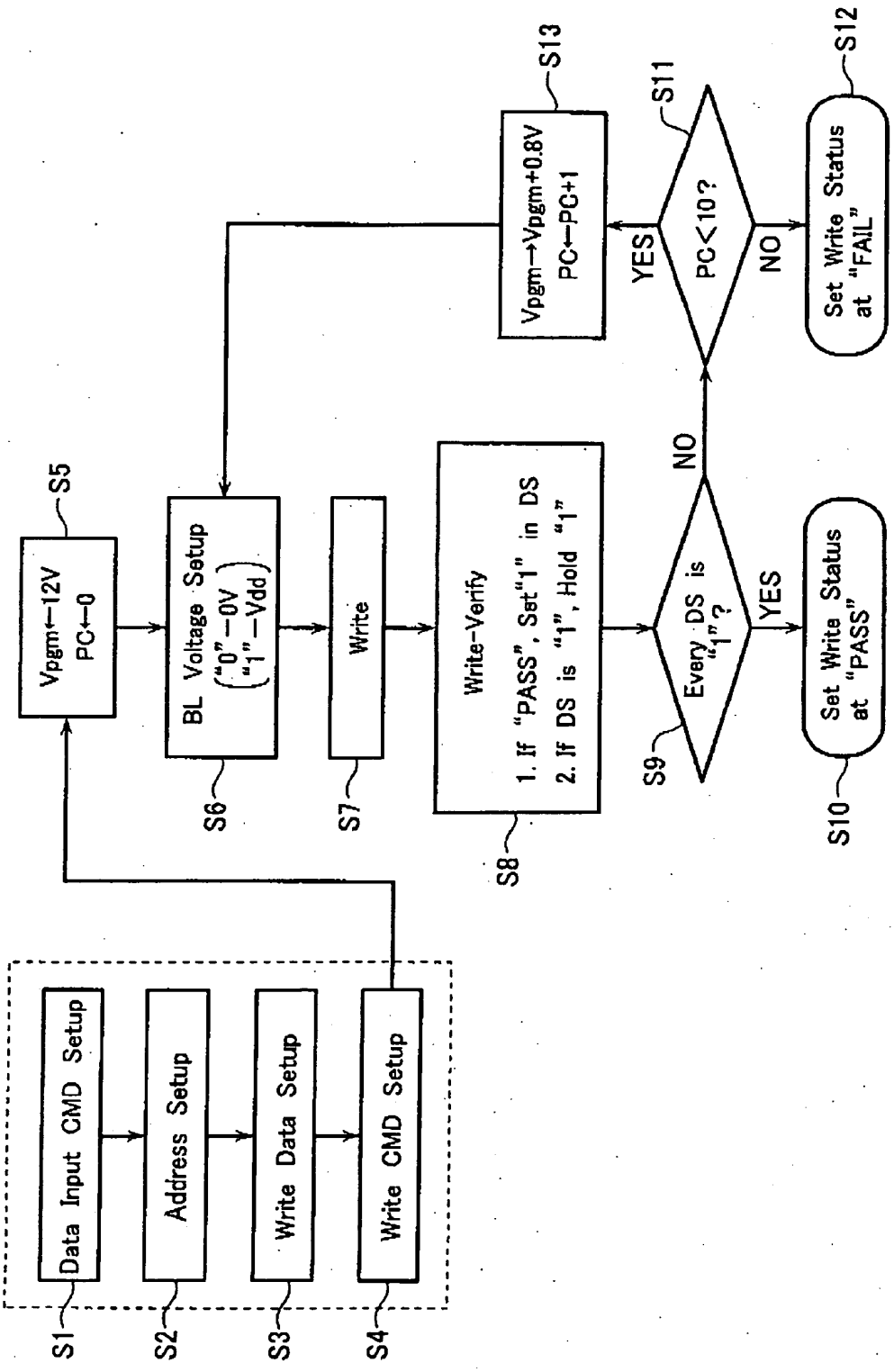
Data Input CMD Setup
Address Setup
Write Data Setup
Write CMD Setup
S1
S2
S3
S4
Vpgm←12V
PC←0
S5
BL Voltage Setup
("0"→0V
"1"→Vdd)
S6
Write
S7
Write-Verify
1. If "PASS", Set "1" in DS
2. If DS is "1", Hold "1"
S8
Every DS is "1"?
S9
YES
NO
Set Write Status at "PASS"
S10
PC<10?
S11
YES
NO
Vpgm→Vpgm+0.8V
PC←PC+1
S13
Set Write Status at "FAIL"
S12

FIG. 13

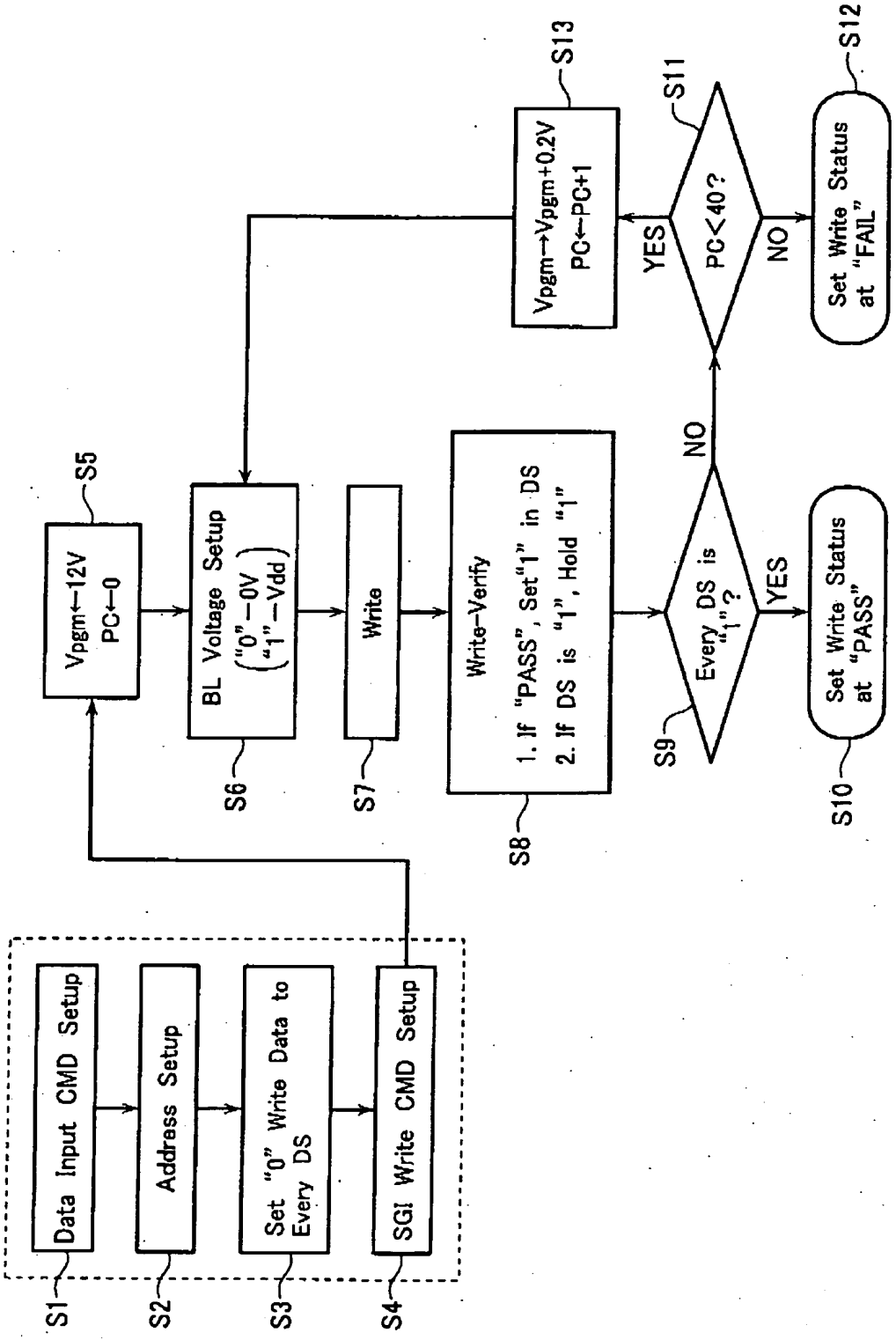
Data Input CMD Setup
Address Setup
Set "0" Write Data to Every DS
SGI Write CMD Setup
S1
S2
S3
S4
Vpgm←12V
PC←0
S5
BL Voltage Setup
("0"→0V
"1"→Vdd)
S6
Write
S7
Write-Verify
1. If "PASS", Set"1" in DS
2. If DS is "1", Hold "1"
S8
Every DS is "1"?
S9
YES
Set Write Status at "PASS"
S10
NO
PC<40?
S11
YES
Vpgm→Vpgm+0.2V
PC←PC+1
S13
NO
Set Write Status at "FAIL"
S12

FIG. 14

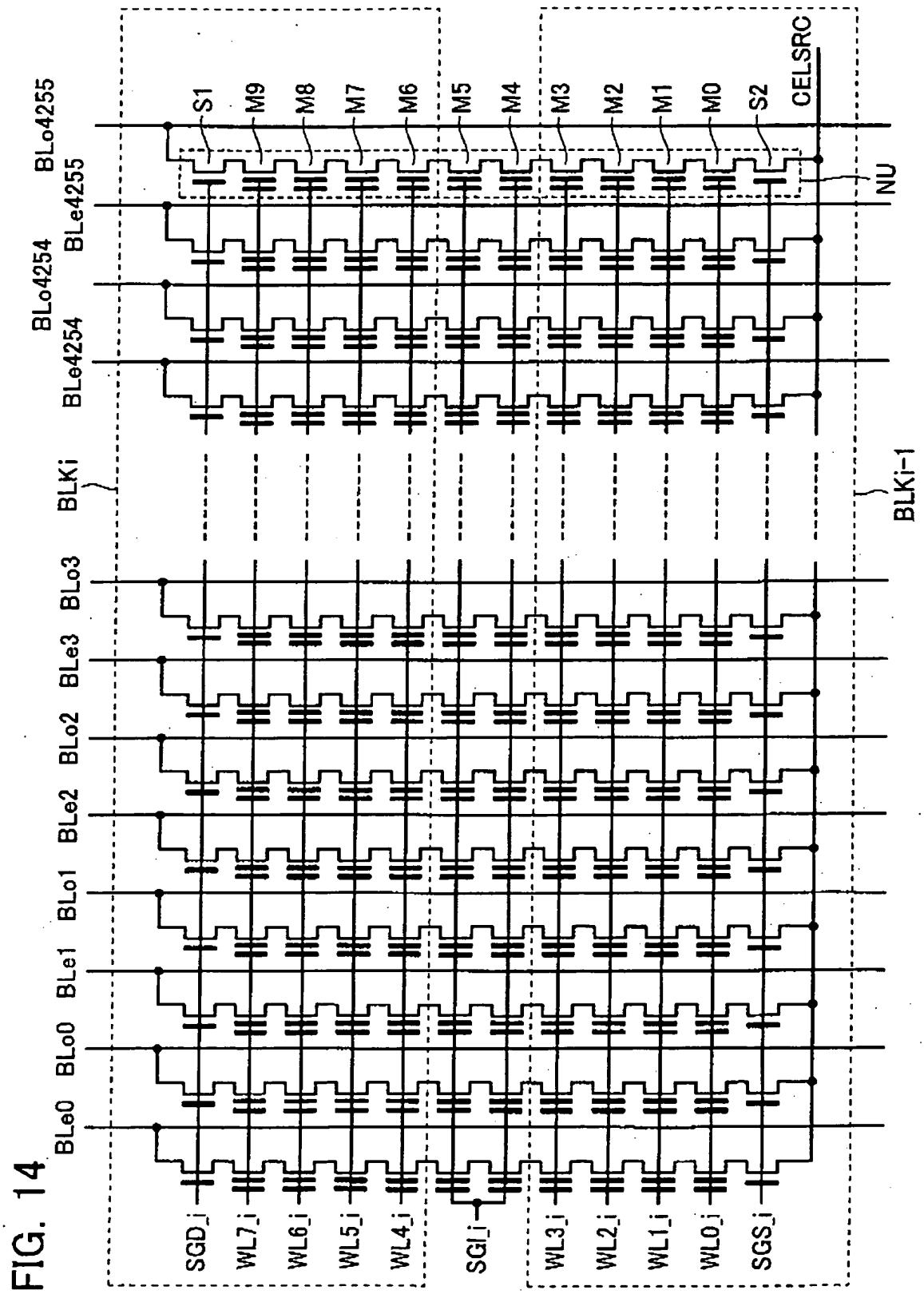
BLo4255
BLe4255
BLo4254
BLe4254
BLKi
BLo3
BLe3
BLo2
BLe2
BLo1
BLe1
BLo0
BLe0
S1
M9
M8
M7
M6
M5
M4
M3
M2
M1
M0
S2
CELSRC
NU
BLKi-1
SGD_i
WL7_i
WL6_i
WL5_i
WL4_i
SGI_i
WL3_i
WL2_i
WL1_i
WL0_i
SGS_i

FIG. 15

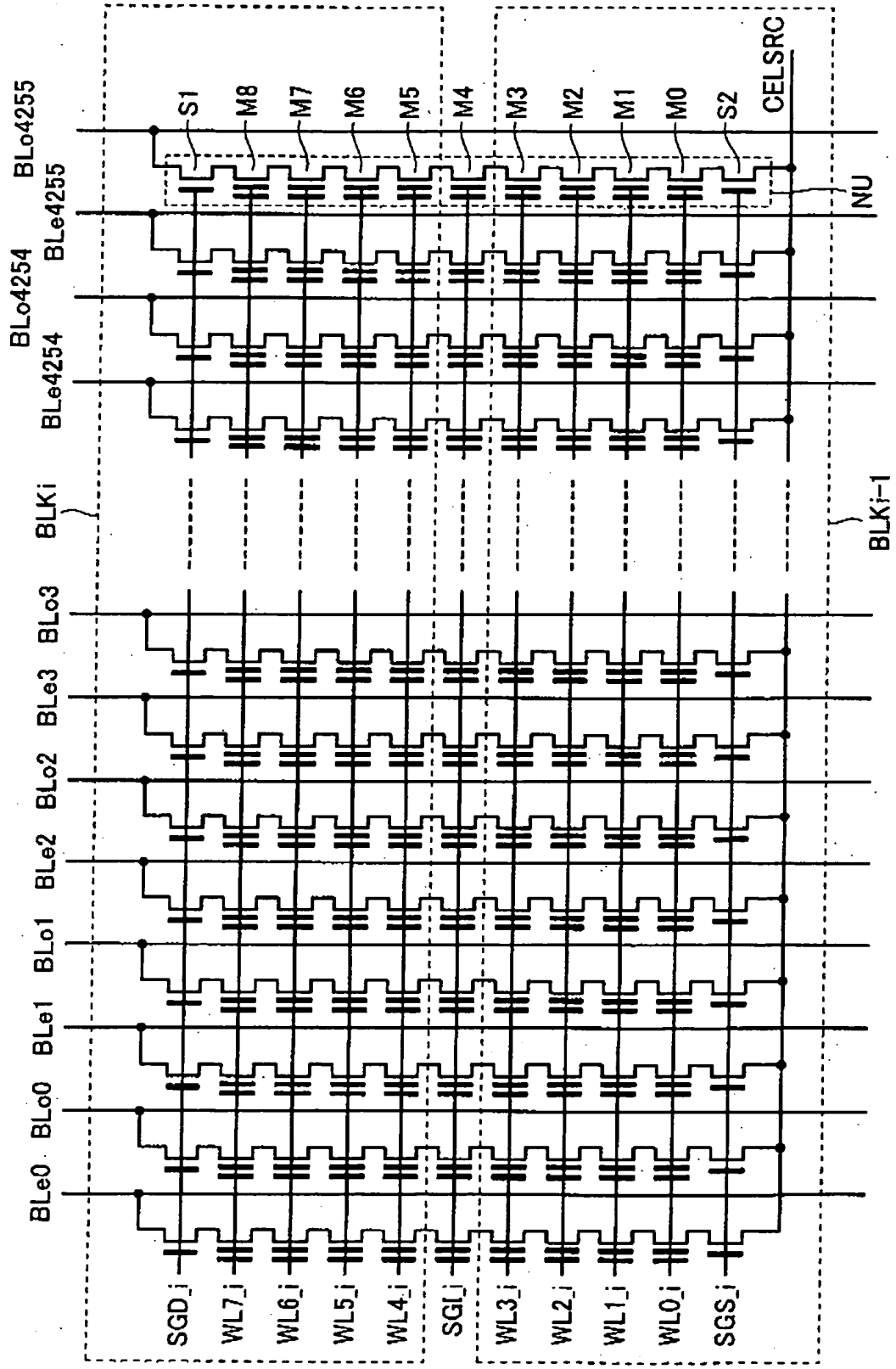
BLo4255
BLe4255
BLo4254
BLe4254
BLKi
BLo3
BLe3
BLo2
BLe2
BLo1
BLe1
BLo0
BLe0
S1
M8
M7
M6
M5
M4
M3
M2
M1
M0
S2
CELSRC
NU
BLKi-1
SGD_i
WL7_i
WL6_i
WL5_i
WL4_i
SGL_i
WL3_i
WL2_i
WL1_i
WL0_i
SGS_i

FIG. 16

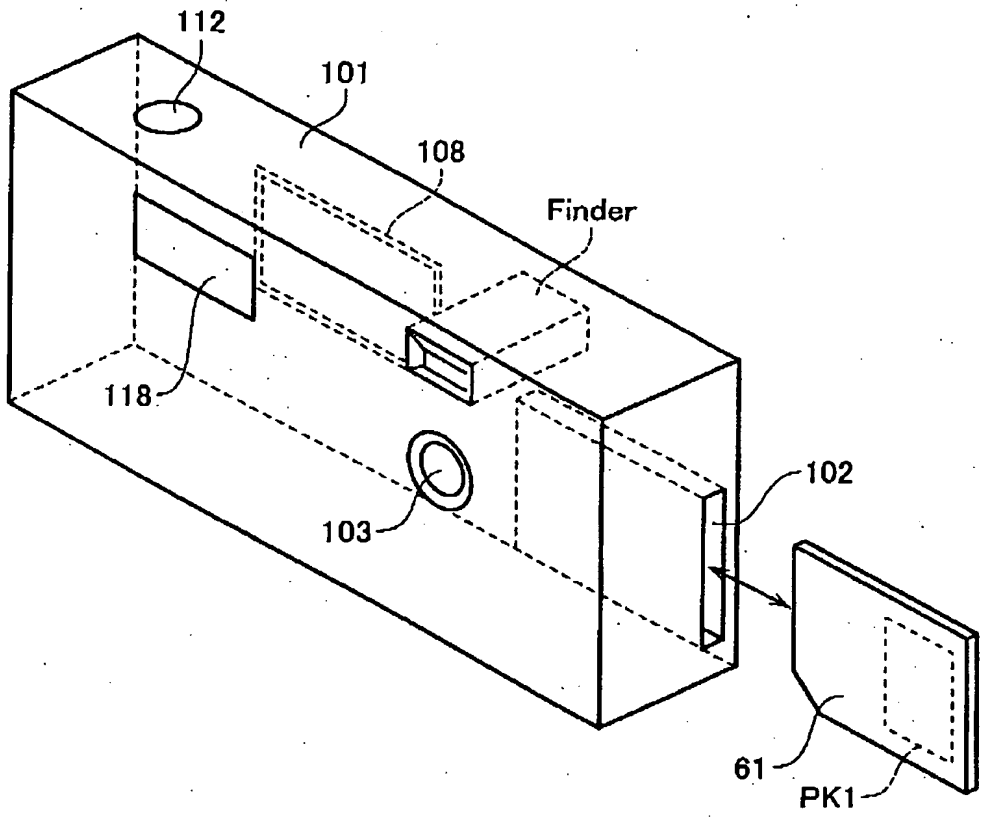

FIG. 17

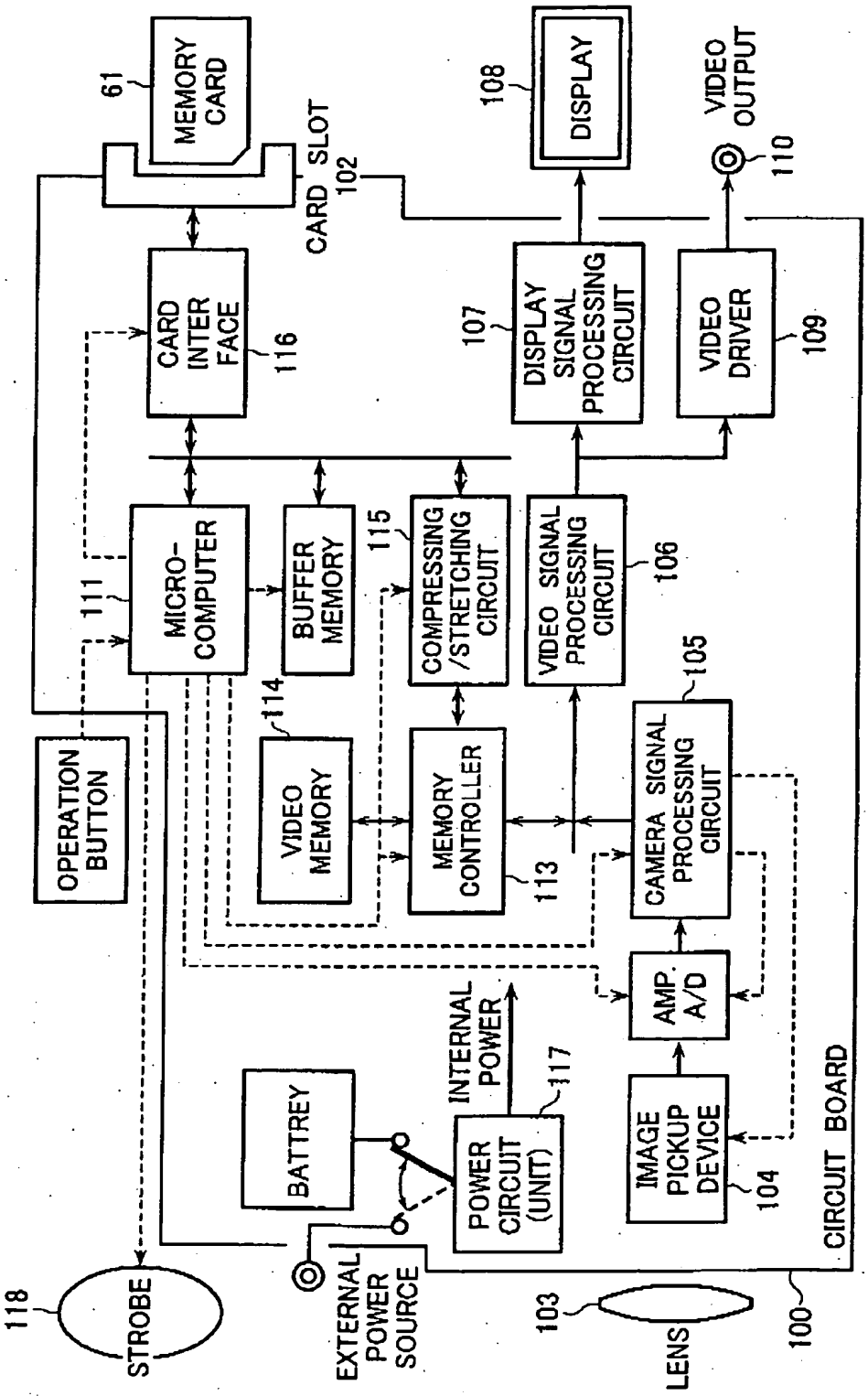
61
MEMORY CARD
CARD SLOT
102
108
DISPLAY
VIDEO OUTPUT
110
CARD INTER FACE
116
107
DISPLAY SIGNAL PROCESSING CIRCUIT
VIDEO DRIVER
109
111
MICRO-COMPUTER
BUFFER MEMORY
115
COMPRESSING /STRETCHING CIRCUIT
VIDEO SIGNAL PROCESSING CIRCUIT
106
105
114
OPERATION BUTTON
VIDEO MEMORY
MEMORY CONTROLLER
113
CAMERA SIGNAL PROCESSING CIRCUIT
AMP. A/D
INTERNAL POWER
117
BATTREY
POWER CIRCUIT (UNIT)
IMAGE PICKUP DEVICE
104
CIRCUIT BOARD
118
STROBE
EXTERNAL POWER SOURCE
103
LENS
100

FIG. 18A

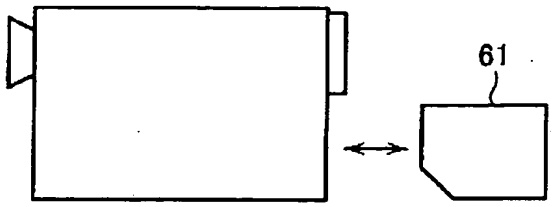

FIG. 18B

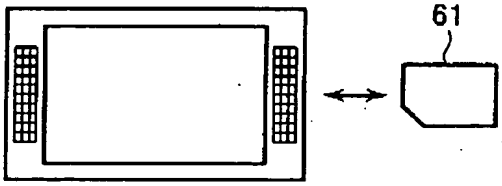

FIG. 18C

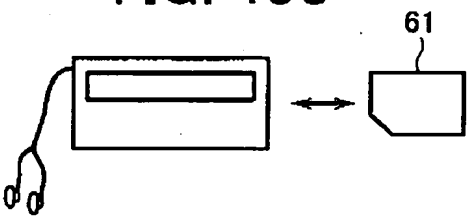

FIG. 18D

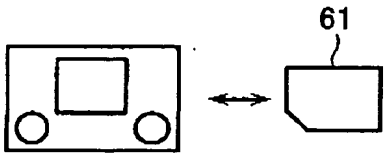

FIG. 18E

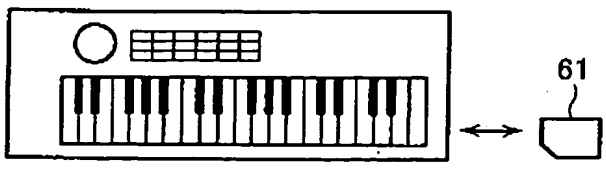

FIG. 18F

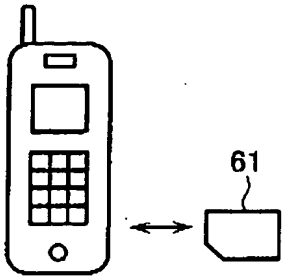

FIG. 18G

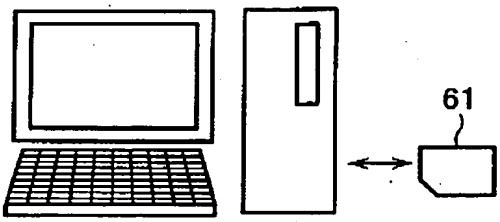

FIG. 18H

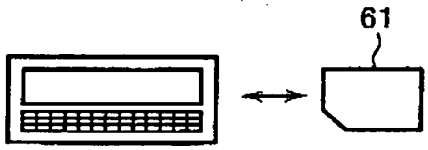

FIG. 18I

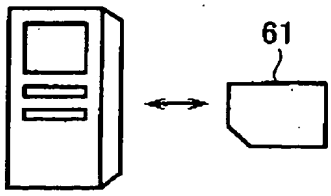

FIG. 18J